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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/798,046	03/11/2004	Von-Kyoung Kim	004-8844	4971

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EXAMINER	
SIEK, VUTHE	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 07/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/798,046	KIM ET AL.	
	Examiner	Art Unit	
	Vuthe Siek	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,10-21,23-29 and 31-37* is/are rejected.

7)☒ Claim(s) *3-9,22 and 30* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application 10/798,046 filed on 3/11/2004. Claims 1-37 remain pending in the application.

Claim Objections

2. Claim 31 is objected to because of the following informalities: "a first plurality of the distinct timing paths". The limitation of "the distinct timing paths" needed clarification in order to avoid claim construction problem. The limitation of "or other magnetic" should be deleted or specified. Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 1, 13, 15, 23, 31 and 36 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

5. As to claim 1 recited, "associating **a first plurality of the distinct timing paths** with **a first set of timing paths**, **individual ones of the first plurality** belonging to **a second set of the timing paths** and including **a first common characteristic**". The claim as recited is not clear. Each of the limitations in bold must be clearly defined in order to avoid claim construction problem. It is confused. Applications are requested to clearly point out where in specification (specific page and lines) and figures.

6. As to claim 15, the recitation of "**a first common characteristic**" needed to be defined; the recitation of "wherein individual ones of the plurality of circuits include at least one circuit element **not present in timing paths** (is it distinct timing paths) **unaltered** for reducing timing violations, **the circuit element being inserted into the plurality of circuits** based at least in part on an improvement to a first timing path of the distinct timing paths" is confused. It appears that the circuit element already being existed in ones of the plurality of circuits, why needed to be inserted and why at least one circuit element not present in timing paths unaltered because the plurality of circuits form distinct timing paths. It is confused. Applications are requested to clearly point out where in specification (specific page and lines) and figures.

7. The above rejections apply to each independent claim 23, 31 and 36.

8. As to claim 13, "fabricating an integrated circuit design including **the replacement circuits**". The replacement circuits needed to be specific in order avoid claim construction problem. Applicants are requested to revise the claims to be precise and indicate to specification with page and lines and drawings.

9. Other dependent claims which are not specifically cited above are also virtually rejected because of the deficiencies of their respective parent claims.

Claim Rejections - 35 USC § 101

10. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 23-26 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. The claims refer to a computer readable encoding or a computer program without storing and executing in a computer readable medium are not statutory.

Claims 31-35 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. Claims 31-35 appear to be to an abstract idea rather than a practical application of the idea. The claims recited do not result in a physical transformation nor does it appear to provide a useful, concrete and tangible result. Thus, claims 31-35 appear non-statutory.

Claim Rejections - 35 USC § 102

11. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

12. Claims 1, 2, 10-21, 23-25, 27-29, 31-34 and 36-37 are rejected under 35 U.S.C. 102(e) as being anticipated by Kovacs et al. (US 2005/0050496 A1).

13. As to claims 1 and 36, Kovacs et al. teach a method for determining or detecting timing violations in an arrangement of components in an IC design (Figs. 1A-C show arrangement of components in an IC design). A timing analysis is performed to determine timing violations in a plurality of timing paths. The timing violations are

distinct timing paths (Fig. 2, 0023; 0027, 0032, 0033). Figs. 1A-C describes two distinct timing paths having timing violations, timing paths 5A and 5B. Kovacs et al. teach identifying a different set of timing paths having timing violations (0033). Similar wire 12D to both timing paths is replaced to optimize the circuit design (to improve timing paths) (0025, 0026, and 0027). The wire 12D is individual ones of the first set of timing paths belonging to a second set of timing paths and including a first common characteristic. The first common characteristic includes same source or component or node or simply wire or interconnection as shown in Figs. 1A-C. Wires are selected and replaced by new wires for reducing timing violations; drivers or circuit components along timing paths having timing violations can also be modified (sizing components, inserting components) to eliminate timing path violations. These teachings are common practice in IC design verification to meet timing requirement or to eliminate time violations.

14. As to claims 15 and 23, Kovacs et al. teach a method for determining or detecting timing violations in an arrangement of components in an IC design (Figs. 1A-C show arrangement of components in an IC design). A timing analysis is performed to determine timing violations in a plurality of timing paths. The timing violations are distinct timing paths (Fig. 2, 0023; 0027, 0032, 0033). Kovacs et al. teach identifying a different set of timing paths having timing violations (0033). Figs. 1A-C describes two distinct timing paths having timing violations, timing paths 5A and 5B. Similar wire 12D to both timing paths is replaced to optimize the circuit design (to improve timing paths). The wire 12D is not present in the timing paths unaltered for reducing timing violations. Fig. 1C shows inserting of new wire 12K to improve timing paths. The first common

characteristic includes same source or component or node or simply wire or interconnection as shown in Figs. 1A-C. Wires are selected and replaced by new wires for reducing timing violations; drivers or circuit components along timing paths having timing violations can be modified (sizing components, inserting components) to eliminate timing path violations. These teachings are common practice in IC design verification to meet timing requirement or to eliminate time violations.

15. As to claims 23 and 27, Kovacs et al. teach a method for determining or detecting timing violations in an arrangement of components in an IC design (Figs. 1A-C show arrangement of components in an IC design). A timing analysis is performed to determine timing violations in a plurality of timing paths. The timing violations are distinct timing paths (Fig. 2, 0023, 0027, 0032, 0033). Figs. 1A-C describes two distinct timing paths having timing violations, timing paths 5A and 5B. Similar wire 12D to both timing paths is replaced to optimize the circuit design (to improve timing paths). The wire 12D is not present in the timing paths unaltered for reducing timing violations. Fig. 1C shows inserting of new wire 12K to improve timing paths as equivalent component for substitution or replacement. The first common characteristic includes same source or component or node or simply wire or interconnection as shown in Figs. 1A-C. The method and system as taught by Kovacs are performed and executed on a computer system using prepared design files representing the IC design. Wires are selected and replaced by new wires for reducing timing violations; drivers or circuit components along timing paths having timing violations can be modified (sizing components, inserting

components) to eliminate timing path violations. These teachings are common practice in IC design verification to meet timing requirement or to eliminate time violations.

16. As to claim 31, Kovacs et al. teach a method for determining or detecting timing violations in an arrangement of components in an IC design (Figs. 1A-C show arrangement of components in an IC design). A timing analysis is performed to determine timing violations in a plurality of timing paths. The timing violations are distinct timing paths (Fig. 2, 0023, 0027, 0032, 0033). Figs. 1A-C describes two distinct timing paths having timing violations, timing paths 5A and 5B. Similar wire 12D to both timing paths is replaced to optimize the circuit design (to improve timing paths). The wire 12D is individual ones of the first set of timing paths belonging to a second set of timing paths and including a first common characteristic. The first common characteristic includes same source or component or node or simply wire or interconnection as shown in Figs. 1A-C. Wires are selected and replaced by new wires for reducing timing violations; drivers or circuit components along timing paths having timing violations can be modified (sizing components, inserting components) to eliminate timing path violations. These teachings are common practice in IC design verification to meet timing requirement or to eliminate time violations.

17. As to claims 10-11, Kovacs et al. teach eliminating timing violations from an IC design (Fig. 2). Kovacs et al. teach various examples of timing delay violations compared to selected threshold delays (0034-0041). The threshold delay can be selected to be higher that the expected worse case delay and lower that the delay value that would guarantee a timing violation. These teachings clearly anticipate the

improvement of timing path includes reducing a maximum timing violation and reducing a minimum timing violation.

18. As to claims 12 and 37, Kovacs et al. teach replacement of wires or circuits to improve or eliminate timing violations of timing paths (0023,0025,0026,0027,and 0031). Wires are selected and replaced by new wires for reducing timing violations; drivers or circuit components along timing paths having timing violations can be modified (sizing components, inserting components) to eliminate timing path violations. These teachings are common practice in IC design verification to meet timing requirement or to eliminate time violations.

19. As to claim 13, Kovacs et al. fabricating IC design after eliminating timing violations (0024).

20. As to claim 14, Figs. 1A-C show preparing the IC design and thereafter performing the improvement (see also Fig. 2).

21. As to claims 2, 16, 18-21, 24, 28 and 33, Kovacs et al. teach Figs. 1A-C show sets of distinct timing paths (first and second) having common characteristic, identified to have a timing violation and the IC design being modified to eliminate the timing violation (Figs. 2, 3, 0032). The common characteristic includes a sequence of devices (devices, wires), an origin of a timing path (clocked device), a destination of a timing path (clocked devices), inclusion of a first net and a first block in a timing path (wires, logics) as shown in Figs. 1A-C.

22. As to claims 17, 25, 29, 32 and 34, Kovacs et al. teach in Fig. 1A-C distinct timing paths (see also 0032) are one set of a plurality of sets of timing paths included in

a second set of timing paths, individual ones of the second set of timing paths having at least one common characteristic. Fig. 1A show sets of distinct timing paths having a common characteristic (original clocked device or sequence of wires or sequence of components).

Allowable Subject Matter

23. Claims 3, 22, 26, 30 and 35 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims and if rewritten to overcome the rejection(s) under 35 U.S.C. 112, second paragraph and 101 when applied, set forth in this Office action. The prior art of record does not teach or fairly suggest associating a second plurality of distinct timing paths with the second set of timing paths, individual ones of the second plurality of distinct timing paths including a second common characteristic, the associating based at least in part on a prioritization of individual ones of the second set of timing paths.

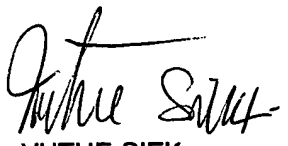
Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vuthe Siek whose telephone number is (571) 272-1906.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on (571) 272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Vuthe Siek



VUTHE SIEK
PRIMARY EXAMINER